IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Group Art Unit of parent application: 2822
Examiner of parent application: POTTER, ROY KARL

In Re PATENT APPLICATION Of:

Applicant	: Naokatsu IKEGAMI	)
Cont. of Appln. Ser. No.	: 10/320,507 filed December 17, 2002	)
Filed	: July 24, 2003	) **INFORMATION**
		) **DISCLOSURE**
For: METHOD OF MANUFACTURING SEMICONDUCTOR DEVICE HAVING THIN FILM SOI STRUCTURE		) **STATEMENT**
Attorney Ref.	: 02DCOAI010-CA	)

July 24 2003

Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is an Information Disclosure Statement submitted in compliance with the timing requirements of 37 C.F.R. § 1.97(b)(3).

Attached are copies of one publication written in English and one publication written in Japanese. These documents are listed on the attached Form PTO-1449. These publications are described and their relevance are explained on pages 2 and 3. Moreover, English language summary for the Japanese publication is also attached.

Since this Information Disclosure Statement is being filed before the mailing of a First Office action on merits, no certification or fee is required, and the requirements of 37 C.F.R. §§ 1.97 and 1.98 are deemed to be fully met as to all documents submitted. Consideration of the submitted documents is respectfully requested.

Respectfully submitted,

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FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	Atty Docket 02DCOAI010-CA	U.S. Application No.: To be assigned
	Applicant Naokatusu IKEGAMI	
	U.S. Filing Date: July 24, 2003	Group To be assigned

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub-Class	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						

FOREIGN PATENT DOCUMENTS

		Document Number	Pub. Date	Country	Class	Sub-Class	Translation
	AL						
	AM						
	AN						
	AO						

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	"Deep Sub-0.1μm MOSFET's with very thin SOI layer for ultra-low power consumption", C-II vol. J81-C-II No. 3, pp 313-319 published in March, 1998 by The Institute of Electronics, Information and Communication Engineers Author : Makoto TAKAMIYA, Yuri YASUDA and Toshiro HIRAMOTO Note: English Summary is attached
	AS	"Optimization of Series Resistance in Sub-0.2 mm SOI MOSFET's", IEEE Electron device letters, Vol. 15, No. 09 Page 363 published in September,1994 Author : Lisa T. Su, Melanie J. Sherony, Hang Hu, James E. Chung and Dimitri A. Antonidis

Examiner	Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.